Key to Midterm Exam S2 Computer Architecture

Duration: 1 hr 30 min

Answer on the answer sheet <u>only</u>.

Do not show any calculation unless you are explicitly asked.

Do not use a pencil or red ink.

Exercise 1 (9 points)

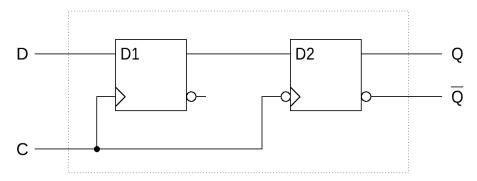
- 1. Convert the numbers given on the <u>answer sheet</u> into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
- 2. Convert the **double-precision** IEEE-754 words given on the <u>answer sheet</u> into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).

Answer the following questions for normalized numbers only and give the result in a power-of-two form.

- 3. For the single precision, what is the smallest number (greater than 0) which, when added to 16, gives a different result from 16?
- 4. For the double precision, what is the smallest number (greater than 0) which, when added to 2^{83} , gives a different result from 2^{83} ?

Exercise 2 (3 points)

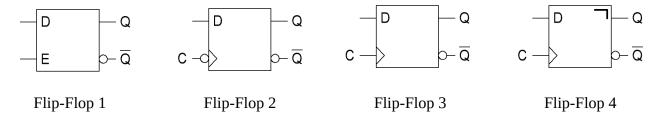
Let us consider the following circuit:



- 1. Complete the timing diagrams shown on the <u>answer sheet</u> (up to the last vertical dotted line).
- 2. If we consider the whole circuit as only one D flip-flop, what type of flip-flop is it?

Exercise 3 (2 points)

Give the type of each flip-flop below (answer on the <u>answer sheet</u>).



Exercise 4 (6 points)

Complete the timing diagrams shown on the <u>answer sheet</u> (up to the last vertical dotted line) for the following circuits.

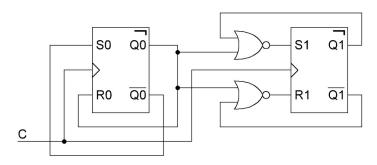


Figure 1

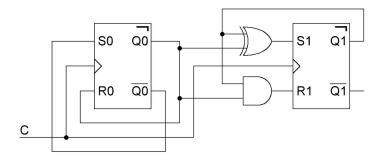


Figure 2

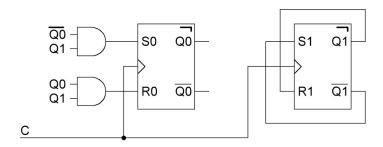


Figure 3

Family name: Group: Group:

ANSWER SHEET

Exercise 1

1.

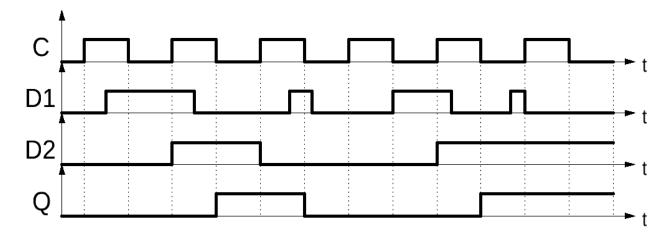
Number	S	E	М
483	0	10000111	11100011000000000000000
84.4375	0	10000101	0101000111000000000000
0.171875	0	01111100	0110000000000000000000

2.

IEEE-754 Representation (base 16)	Associated Representation
3A44 0000 0000 0000	5 × 2 ⁻⁹³
7FF0 0000 0000 0000	+∞
000A D000 0000 0000	173 × 2 ⁻¹⁰³⁰
7FF1 0000 0000 0000	NaN

3. 2 ⁻¹⁹	4. 2 ³¹

Exercise 2



Type of flip-flop:

Master-slave D flip-flop

Exercise 3

Flip-Flop	Type of flip-flop		
1	Gated D latch		
2	Negative-edge-triggered D flip-flop		
3	Positive-edge-triggered D flip-flop		
4	Master-slave D flip-flop		

Exercise 4

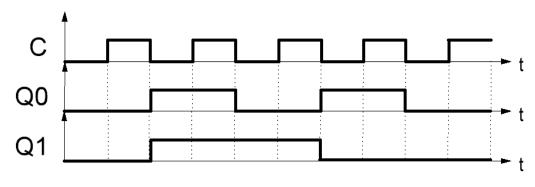


Figure 1

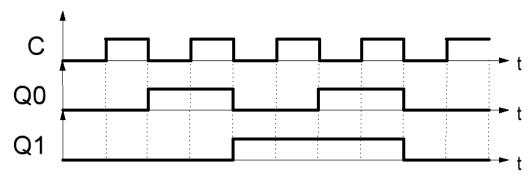


Figure 2

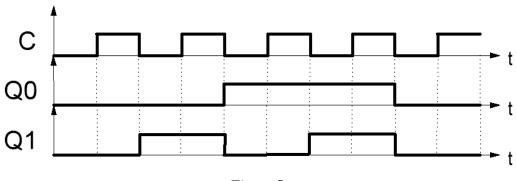


Figure 3