Final Exam S2
Computer Architecture

Duration: 1 hr 30 min

Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use a pencil or red ink.

Exercise 1 (4.5 points)

The table shown on the answer sheet gives the sequence of a counter we want to design. This counter should be made up of D flip-flops.

1. Complete the table shown on the answer sheet.
2. Write down the most simplified expressions of *D* for each flip-flop. **Complete the Karnaugh maps for the solutions that are not obvious (circles included)**. An obvious solution does not have any logical operations apart from the complement (for instance: D0 = 1, D1 = $\overline{Q0}$). If possible, simplify with the exclusive OR operator.

Exercise 2 (4 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The capacities (in bits) of these devices are 4 Mib, 64 Kib, 8 Kib and 1 Kib respectively. The microprocessor has a 24-bit address bus (the address bits are numbered from *A0* to *A23* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space, followed by the RAM, **P1** and **P2**.

1. Calculate the size of the address buses for each device.

For the following questions, the linear-decoding technique must be used.

2. Which address bits are required to select the devices?
3. Write down an expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.
4. Give the lowest and highest addresses for each device. (Use the 6-digit hexadecimal representation.)

Exercise 3 (4 points)

1. Wire the flip-flops (figure 1) in order to design a **modulo-13 asynchronous down counter**.
2. Wire the flip-flops (figure 2) in order to design a **modulo-4 synchronous up counter**.

Exercise 4 (4 points)

1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the base-10 following form: $k \times 2^n$ where k and n are integers (either positive or negative).

Exercise 5 (3.5 points)

Answer the questions on the answer sheet.

Family name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

1.

Q2	Q1	Q0	D2	D1	D0
1	1	1			
1	0	1			
1	0	0			
0	1	1			
0	1	0			
0	0	1			
0	0	0			

2.

		Q1 Q0			
	D0	**00**	**01**	**11**	**10**
Q2	**0**				
	1				

D0 =

		Q1 Q0			
	D1	**00**	**01**	**11**	**10**
Q2	**0**				
	1				

D1 =

		Q1 Q0			
	D2	**00**	**01**	**11**	**10**
Q2	**0**				
	1				

D2 =

Exercise 2

1. ROM:

   RAM:

   P1:

   P2:

2. Device-selection bits:

3. CS_{ROM} = CS_{P1} =

   CS_{RAM} = CS_{P2} =

4.

Device	Lowest Address	Highest Address
ROM		
RAM		
P1		
P2		

Exercise 3

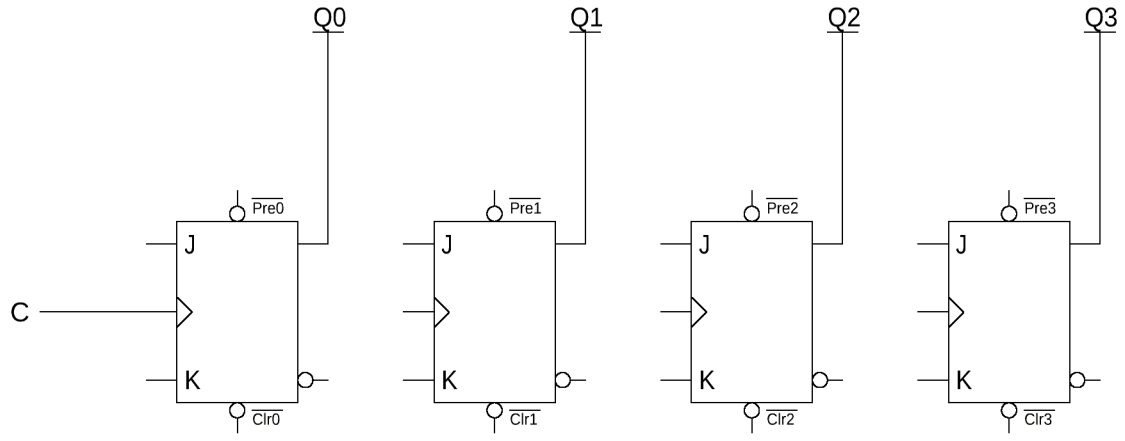

Figure 1

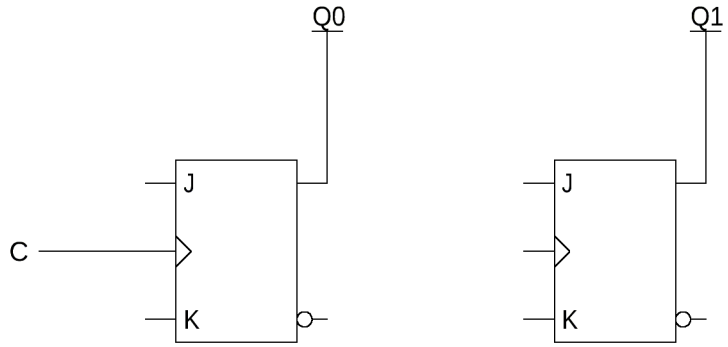

Figure 2

Exercise 4

1.

Number	S	E	M
428			
51.078125			

2.

IEEE-754 Representation	Associated Representation
4354000000000000_{16}	
0010100000000000_{16}	

Exercise 5

Question about memory devices	**Answer**
How can we connect memory devices in order to enlarge the depth?	
A memory has a width of 4 bits and a capacity of 64 KiB. How many address lines does this memory have?	
A memory has an 8-bit data bus and a 15-bit address bus. In a power of two, what is the capacity in bits of this memory?	
An **M1** memory has an 8-bit data bus and a 16-bit address bus. Two **M1** memories are connected in series to build an **M2** memory. What is the size of the address bus of the **M2** memory?	

Feel free to use the blank space below if you need to: